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APPLICATION FOR U.S. LETTERS PATENT

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SEMICONDUCTOR WITH AN IMPROVED READ DEVICE AND OPERATIONAL MODE ASSOCIATED THEREWITH

Cross-Reference to Related Application

[001] This application claims the benefit of priority under 35 U.S.C. § 365(c) as a continuation of International Application No. PCT/DE02/02715, filed July 24, 2002, which published in German on February 20, 2003 as WO 03/015103.

Field of Invention

[002] The present invention relates to floating gate memories and, in particular, to a drive circuit and a differential read concept for non-volatile one-transistor floating gate memories.

Background of the Invention

[003] In a floating gate memory, the information is stored by changing the quantity of charge on the floating gate of the memory transistor by means of one or more high voltages, with the result that the memory transistor conducts or blocks current under specific conditions. During the read-out of the cell, the control gates of all the memory transistors that are not to be read are held at a low potential (e.g., 0 volts), while the control gate of the cell to be read is brought to a higher read potential (e.g., 1.8 volts). A problem in the art is that memory transistors with a

positive potential on the floating gate on the same signal line as the memory transistor to be evaluated can also contribute to a read current with a low control gate voltage and, thus, corrupt the read result for the memory cell to be read.

[004] To date, the problem has been solved in that, in cells which are intended to have a conducting information state, the floating gate potential has been set so low that no current flows through them in the non-selected state. A disadvantage of this solution is that the high voltage has to be applied in pulsed fashion, and measured after each pulse to determine whether the cell has already reached the correct floating gate potential. Moreover, for the case where an excessively high floating gate potential is inadvertently reached, it is necessary to provide a recovery mechanism. In addition, the low floating gate potential in the cells reduces the read current and thus the read speed and restricts the read window.

[005] In particular, there is a need for a floating gate memory in which these problems are avoided. The present invention satisfies these and other needs, as set forth in the following description.

Summary of the Invention

[006] In accordance with one aspect of the invention, a memory cell comprises memory transistors arranged in groups, with each group being assigned a selection transistor. A drive circuit is connected to the memory cell, so that the memory cell can be selected and data can be read and written. The groups of memory transistors can comprise 16 to 32 transistors and can also be arranged in rows and columns.

[007] In accordance with another aspect of the invention, a method for operating a drive circuit comprises the steps of opening a selection transistor for a group of memory transistors, while the gate terminals of the memory transistors are at a low potential. While in this condition a first current for each row or column to be read is measured and stored. The method further comprises raising the potential of a memory transistor gate terminal of a row or column to be read and comparing a resulting second current with the first current.

[008] These and other aspects, features, steps and advantages can be further appreciated from the accompanying drawings and description of certain illustrative embodiments.

Brief Description of the Drawing Figures

[009] Figure 1 is a portion of a memory cell which embodies the invention; and

[0010] Figure 2 is the memory cell portion of Figure 1 with a memory transistor selected.

Detailed Description of the Illustrative Embodiments

[0011] The invention arranges a drive circuit and memory cells to avoid the problems known in the prior art. In an embodiment of the invention a selection transistor 2 for a group of memory cells 1, preferably composed of 16 to 32 memory cells, is inserted into the leads to the memory cells. Since the memory cells in a memory are usually arranged in a matrix-like grid and subdivided into rows and columns, it is assumed, in order to simplify the description, that the group of memory cells, in a preferred exemplary embodiment, forms a row group. However, the arrangement according to the invention may correspondingly be provided if a column group is

intended to be addressed in this way, or the designations of rows and columns are interchanged with one another.

[0012] For reading, first the selection transistor 2 for a row group is opened, while the control gates of all other rows are at low potential, and the current for each column to be read which leads through said row group is measured and stored. In a second step, the control gate (or control gates) of the row to be read is/are brought to the higher read potential and the resulting current is compared with the previous current. According to the invention, a leakage current through the non-selected cells is not a disturbance, because only the difference between the current with and without a selected cell is taken as a benchmark for a decision about the information of the memory cell.

[0013] A preferred embodiment of the invention is described below with reference to Figures 1 and 2, which illustrate the two steps of the read operation using a detail from the memory cell arrangement.

[0014] Figure 1 illustrates a detail from a memory cell array in which the memory transistors 1 can be jointly selected in a groupwise manner in each case by means of a selection transistor 2. Figure 1 depicts two such groups of 16 to 32 memory transistors, which are each connected to a selection transistor 2. The selection transistor 2 depicted at the top in Figure 1 has been opened by the application of a potential of typically 1.8 volts to the gate terminal 3, so that the associated memory transistors can be read. Because all these memory transistors are still blocked with a gate potential of 0 volts, initially only the output current I1 flows.

[0015] Figure 2 illustrates the next step of the read operation, in which the gate terminal 5 of a selected memory transistor 4 is put at typically 1.8 volts. The memory content of this transistor can therefore be read out, so that now an output current I2 flows.

[0016] Thus, while there have been shown, described, and pointed out fundamental novel features of the invention, it will be understood that various omissions, substitutions, and changes in the form and details of the devices illustrated, and in their operation, may be made by those skilled in the art without departing from the spirit and scope of the invention. Substitutions of elements from one described embodiment to another are also fully intended and contemplated. It is also to be understood that the drawings are not necessarily drawn to scale, but that they are merely conceptual in nature. The invention is defined solely with regard to the claims appended hereto, and equivalents of the recitations therein.